REMARKS

I. Amendments to the Specification

By this amendment, Applicant has corrected a typographical error on page 2 of the specification.

II. Amendments to the Claims

By this amendment, Applicant has amended claim 4, canceled claim 5, and added new claims 6-8. Claim 4 has been amended to correct a typographical error. Claims 1-4 and 6-8 are currently pending. Of these, claims 1 and 6 are independent.

A. Claim Rejections - 35 U.S.C. § 102(b)

Claims 1-5 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Japanese patent application publication number 08-293159 to Matsumoto et al. ("Matsumoto")[1]. Of these claims, the Examiner's rejection of claim 5 has been rendered moot by Applicant's cancellation of claim 5.

Claim 1 recites, among other things: "a detection section which detects whether or not a voltage of one of the right and left signal channel terminals is substantially equal to a ground voltage." Matsumoto fails to teach or suggest at least this element of claim 1.

The Office Action states that Matsumoto discloses this element in paragraphs 0029-0030 (See Office Action, page 2). However, in paragraph 0029, Matsumoto

[1] The Office Action contains a number of statements reflecting characterizations of the related art and the claims. Regardless of whether any such statement is identified herein, Applicant declines to automatically subscribe to any statement or characterization in the Office Action.

discloses that a controller 18 compares a voltage of the right and left signal channels (VLT and VRT) to a predetermined threshold value (VTH). Moreover, in columns 2 and 3 of the table in Figure 2, Matsumoto discloses comparing VRT and VLT to VTH to determine whether they are greater than or less than VTH, not whether they are equal to VTH. Thus, Matsumoto does not disclose "detect[ing] whether or not a voltage of one of the right and left signal channel terminals is *substantially equal* to a ground voltage."

Moreover, although Matsumoto does not appear to disclose an expected voltage level for VLT and VRT in the written description, the voltage levels of VLT and VRT (at terminals 18a and 18b in Figure 1), are non-zero. This is the case because resistors R2 and R4 (in Figure 1), from which VLT and VRT are derived, form voltage divider circuits in conjunction with resistors R1 and R3, respectively. Moreover, since a power supply voltage VPIP is applied to the voltage dividers, voltages VLT and VRT are obtained by dividing the voltage VPIP. Thus, voltages VLT and VRT are clearly non-zero voltages. Therefore, the disclosure of Matsumoto cannot constitute "a detection section which detects whether or not a voltage of one of the right and left signal channel terminals is substantially equal to a *ground voltage*," as required by claim 1. Since Matsumoto fails to teach each and every element of claim 1, claim 1 is not anticipated by Matsumoto.

Independent claim 6, although of different scope, also requires a detection section that includes features corresponding to those of claim 1 discussed above. Therefore, Applicant respectfully submits that claim 6 is also not anticipated by Matsumoto for at least the reasons discussed above with respect to claim 1.

Applicant further submits that claims 2-4 and 7-8 each depend from one of allowable independent claims 1 and 6 and are therefore allowable.

Accordingly, Applicant respectfully requests that the Examiner withdraw the rejection under 35 U.S.C. § 102(b).

Conclusion

In view of the foregoing amendments and remarks, Applicant respectfully requests reconsideration of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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